Antonio Ristevski

(586) 229-9535 | antonioristevsk@oakland.edu

CAREER FOCUS

Dedicated and driven engineer focused on building a career in FPGA design and embedded systems. Experienced in Controller Area Network (CAN) protocol, microcontroller programming, and project management. Possesses strong communication, problem-solving, and leadership skills, with the ability to thrive in fast-paced, challenging environments.

EDUCATION

Bachelor of Science in Engineering, *Computer Engineering* **GPA: 3.76**
Oakland University, Rochester MI *Expected Graduation December 2025*

EXPERIENCE

Formula SAE Electrical Director **May 2024 – Present**

- Integrated over **23** sensors into the data acquisition system, enhancing the team's validation capabilities.
- Overseeing the development and execution of **40+** projects across various stages and levels of priority.
- Ensuring the reliability of the electrical subsystem through comprehensive harness inspections and sensor validation.
- Collaborating with industry leaders in motorsports to expand the team's technical expertise and innovation.
- Managing a **$7,500** budget for electrical components and ensuring cost-effective solutions while maintaining high standards of performance and reliability.
- Added **6** steps to the harness design process to innovate the manufacturing process and reliability of the harness.

Formula SAE Software and Data Lead **May 2023 – May 2024**

- Increased data collection efficiency **by 52%,** significantly reducing driver wait time and optimizing track performance.
- Led a team of **5+** engineers in developing data analysis software to process analog and digital signals from PE3.
- Worked closely with subsystem leads to determine data requirements, utilizing sensors and data collection tools such as NEO VI Fire 3, thermocouple boxes, and GPS modules to optimize and validate system performance.
- Performed signal testing, sensor configuration, and data validation using Vehicle Spy 3 and oscilloscopes.

WORK EXPERIENCE

High-Performance Hardware Intern, *Intrepid Control Systems* **May 2024- August 2024**

- Integrated 128-bit AES encryption into FPGA hardware for enhanced security.
- Analyzed FPGA boot time during power cycles using oscilloscopes.
- Developed LED control patterns for the Galaxy 2 user interface.

FORMULA SAE PROJECTS

First-Year Recruitment and Management Proposal

- Developed an email outreach strategy to engage first-year students, capitalizing on the team's status as the largest student organization at Oakland University.
- Adopted a personalized approach to strengthen relationships and bridge the social gap within the team's hierarchy.
- Proposed a structural reorganization of the team's management to enhance support for the new retention strategy.

Radio Lap Timer

- Implement Wi-Fi telemetry to communicate between four Arduino Nanos for tracking vehicle times.
- Design lap timer PCB to reduce power sources with DC-to-DC boost converters from 5V to 24V.

Dyno Harness 3D Design, 2D Design, and Layup

- Completed over **10** iterations of 3D harness designs to optimize wire layout, lengths, and splice points.
- Wire gauge calculations based on voltage drop percentage calculations.

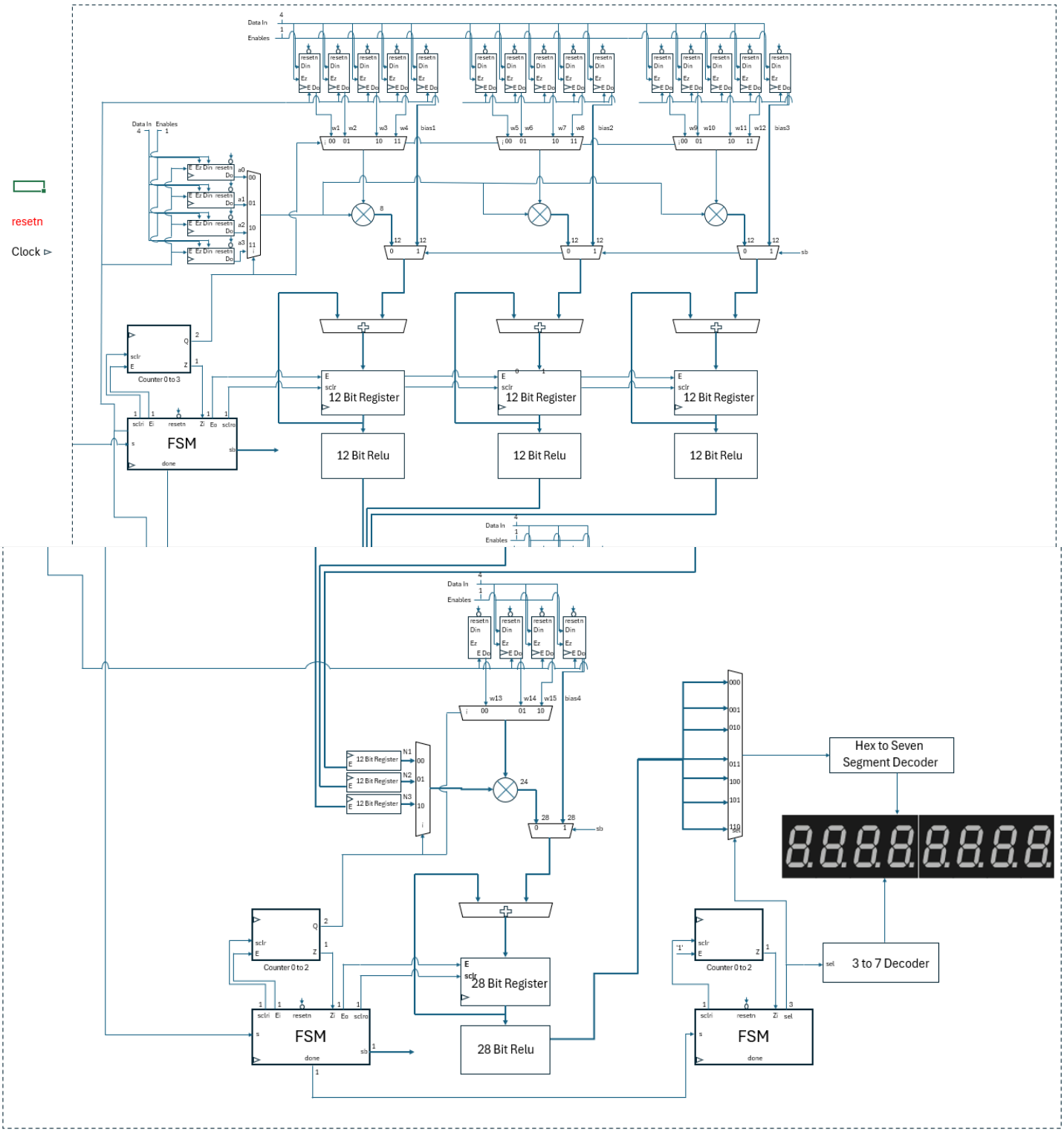
RELEVANT PROJECTS

Neural network on an FPGA.

- Designed a neural network with 4 inputs, 3 hidden neurons, and 1 output.
- Designed **40+** components for the FPGA circuit (design below).

TECHNICAL SKILLS

- Software: Vehicle Spy | PE3 Monitor | Git | Race Render | Catia V5 | ESP-IDF | SolidWorks
- Programming Languages: VHDL | C/C++ | MATLAB
- Other: CAN Protocol | UART | Multimeters | Oscilloscopes | Function Generators


resetn
Clock
Data In
Enables
Counter 0 to 3
FSM
12 Bit Register
12 Bit Relu
Counter 0 to 2
28 Bit Register
28 Bit Relu
Hex to Seven Segment Decoder
3 to 7 Decoder